VERSION WITH MARKINGS TO SHOW CHANGES MADE

11. (AMENDED) An integrated circuit comprising:

means for generating a test signal having a predetermined pulse width in response to a control input; and

means for predicting failure of part or all of said integrated circuit in response to said test signal.

12. (AMENDED) A method for predicting failure of an integrated circuit prior to life testing comprising the steps of:

(A) entering a test mode;

(B) measuring an operation of said integrated circuit in response to a test signal having a predetermined pulse width and generated on said integrated circuit in response to a control input; and

(C) detecting failure of said operation.

21. (NEW) The integrated circuit according to claim 1, wherein said test circuit is further configured (i) to generate said test signal having said predetermined pulse width when in a first mode and (ii) to pass said control input as said test signal when in a second mode.

22. (NEW) The integrated circuit according to claim 21, wherein said test circuit is further configured to enter said first mode in response to a predetermined sequence of input signals.

23. (NEW) The integrated circuit according to claim 1, wherein said test circuit comprises:

a first circuit configured to generate said test signal in response to said control input and a control signal; and

a second circuit configured to generate said control signal in response to a plurality of input signals.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an integrated circuit comprising a test circuit that may be configured to generate a test signal having a predetermined pulse width in response to a control input. The test signal generally tracks process corners of the integrated circuit and may be used to predict a failure of the integrated circuit.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 2 and 3 and in the specification as originally filed, for example, on page 5, line 10 through page 7, line 18. Support for new claim 21 can be found in the specification as originally filed, for example, on page 6, line 16 through page 7, line 9. Support for new claim 22 can be found in the specification as originally filed, for example, on page 7, lines 10-18. Support for new claim 23 can be found in the drawings as originally filed, for example, on FIG. 2 and in the specification as originally filed, for example, on page 5, line 10 through page 7, line 18. As such, no new matter has been added.

IN THE DRAWINGS

The objection to the drawings has been obviated by appropriate amendment and should be withdrawn. A new drawing for FIG.1 is submitted herewith showing the changes requested by the Examiner in red. Support for the changes can be found on the upper abscissa of FIG. 1 as originally filed. As such, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the content of the Abstract has been obviated by appropriate amendment and should be withdrawn. The word "comprising" has been replaced with "includes". The objection to the length of the Abstract is respectfully traversed and should be withdrawn. 37 CFR 1.72 provides "[t]he abstract in an application ... may not exceed 150 words in length." The present Abstract does not exceed 150 words. Furthermore, the present Abstract would enable the USPTO and the public generally to determine **quickly** from a **cursory inspection** the **nature and gist** of the technical disclosure. As such, the present Abstract is believed to be fully compliant with 37 CFR 1.72 and MPEP §608.01(b) and the objection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-20 under 35 U.S.C. §103(a) as being obvious over Ahmad et al. '400 (hereinafter Ahmad) in view of Gascoyne '547 (hereinafter Gascoyne) and Agrawal et al. '163 (hereinafter Agrawal) is respectfully traversed and should be withdrawn.

Ahmad is directed to a semiconductor array having a built-in test circuit for wafer level testing (Title). Gascoyne is directed to a process monitor circuit (Title). Agrawal is directed to an FPGA integrated circuit having embedded SRAM memory block and interconnect channel for broadcasting address and control signals (Title). Ahmad, Gascoyne and Agrawal, alone or in combination, do not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Specifically, the presently claimed invention (claim 1) provides a test circuit configured to generate a test signal having a predetermined pulse width in response to a control input, where the test signal tracks process corners and can be used to predict a failure of an integrate circuit. Claims 11 and 12 include similar recitations. Despite the position taken in the Office Action (see page 3, lines 13-16 of the Office Action), Ahmad does not disclose or suggest a **test circuit configured to generate a**

test signal having a predetermined pulse width in response to a control input, where the test signal tracks process corners and can be used to **predict** a failure of an integrated circuit, as presently claimed. In particular, assuming, *arguendo*, that the on-chip self test circuitry of FIG. 2 of Ahmad is similar to the presently claimed test circuit and the test enable signal 53 is similar to the presently claimed test signal (as suggested on page 3, line 14 of the Office Action and for which Applicants' representative does not necessarily agree), Ahmad does not disclose a test circuit configured to generate a test signal, as presently claimed.

Specifically, the on-chip self test circuitry of Ahmad **does not generate** the test enable signal 53 (see FIG. 2 and column 6, lines 18-21 of Ahmad). Furthermore, the test enable signal 53 is not used to **predict** a failure of the integrated circuit devices on the wafer. Rather, the test enable signal 53 of Ahmad enables the on chip self test circuitry of Ahmad to record the time of a failure that has already occurred (see column 2, lines 25-54 of Ahmad). Furthermore, Ahmad does not disclose or suggest a test signal having a predetermined pulse width generated in response to a control input, where the test signal tracks process corners and can be used to predict failure of an integrated circuit, as presently claimed (see page 3, lines 17-20 of the Office Action).

Despite the suggestion in the Office Action (see page 4, lines 15-17 of the Office Action), Gascoyne and Agrawal do not cure

the deficiencies of Ahmad. Specifically, the Office Action fails to provide factual evidence or a convincing line of reasoning to support the position that Gascoyne and Agrawal, alone or in combination, disclose or suggest a test signal having a predetermined pulse width generated in response to a control input, where the test signal tracks process corners and can be used to predict failure of an integrated circuit, as presently claimed (see page 4, lines 1-4 of the Office Action). Therefore, the Office Action has failed to meet the Office's burden to factually establish a *prima facie* case of obviousness and the rejection should be withdrawn (MPEP §2142).

Furthermore, the statement on page 4, lines 12-17 of the Office Action that because "a person of ordinary skill in this art would be familiar with prior art techniques for testing of semiconductor devices in general and techniques for providing test inputs in particular, at the time of the invention, it would have been obvious for a person of ordinary skill in the art to have combined the teachings of Ahmad, Gascoyne and Agrawal to arrive at the [presently claimed] invention" fails to establish a *prima facie* case of obviousness (see MPEP §2143.01). Specifically, the level of skill in the art cannot be relied upon to provide the suggestion or motivation to combine references (MPEP §2143.01, citing Al-Site Corp. v. VSI Int'l Inc., 50 USPQ2d 1161 (Fed. Cir. 1999)). As such, the statement on page 4, lines 12-17 of the Office Action is

not sufficient to establish a *prima facie* case of obviousness (see MPEP §2143.01) and the rejection should be withdrawn.

Furthermore, the position taken in the Office Action that it would have been obvious for a person of ordinary skill in the art to have combined the teachings of Ahmad, Gascoyne and Agrawal to **arrive at the presently claimed invention** clearly evidences the use of hindsight in the assembly of the cited references to support the obviousness rejection. "It is improper, in determining whether a person of ordinary skill would have been led to [a] combination of references, simply to '[use] that which the inventor taught against its teacher'" (In re Lee, 61 USPQ 2d 1430, 1434 (Fed. Cir. 2002) citing W.L. Gore v. Garlock, Inc.). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the conclusory statement on page 4, lines 18-20 of the Office Action that "[t]he suggestion [or] motivation for doing so would have been that built-in self test (BIST) circuits are more the norm than an exception in most modern integrated circuit architecture, including in SRAMs" is not adequate to support an obviousness type rejection (see In re Lee at 1433-1434). The factual question of motivation is material to patentability and cannot be resolved on subjective belief and unknown authority. As such, the statement on page 4, lines 18-20 of the Office Action is not sufficient to establish a *prima facie*

case of obviousness (see In re Lee) and the rejection should be withdrawn.

Furthermore, the position that Ahmad teaches a specific type of a circuit while Gascoyne and Agrawal teach variations for test signal input and control and that combining the different techniques is a matter of engineering design choice (see page 4, line 20-page 5, line 2 of the Office Action) fails to provide the required reasoning supporting the position that combining the different techniques is a matter of design choice, and therefore obvious (see In re Chu, 36 USPQ 2d 1089 (Fed. Cir. 1995)). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-10 and 13-20 depend either directly or indirectly from claims 1 and 12 which are believed to be fully patentable over the cited references. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Newly presented claims 21-23 depend, either directly or indirectly, from claim 1 and are believed to be fully patentable over the cited references.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

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